A RECEIVER

BACKGROUND OF THE INVENTION

[0001]

5 [Technical Field]

The present invention relates to a receiver for regenerating a signal wave from a received wave, and in particular to a receiver for regenerating a signal wave via digital signal processing.

10 [0002]

[Related Art]

Conventionally, an AM receiver of the superheterodyne system shown in Fig. 3 is known as a receiver for receiving a broadcast wave transmitted from a broadcast station and 15 regenerating a signal wave in the audio frequency band.

[0003]

The AM receiver regenerates a signal wave S_{AF} via analog signal processing. The receiver supplies the AM broadcast wave S_{AF} received by an antenna 1 to a frequency converter 3 via a 20 high-frequency amplifier 2 and mixes the signal with a channel selection signal S_o of the local oscillation frequency from a local oscillator 4 in order to frequency-convert the signal to a signal of the intermediate frequency (455 kHz), hereinafter referred to as an IF signal. The AM receiver removes unwanted 25 frequency components by passing the frequency-converted IF

1

signal S_{IF} through a band-pass filter 5 in the intermediate frequency band, amplifies the resulting signal via a gain control intermediate frequency amplifier 6, removes external noises via a noise clamping circuit 7, then detects the signal via

5 a detection circuit 8 to regenerate a signal wave S_{AF} in the audio frequency band. The AM receiver voltage-splits the signal wave S_{AF} via fixed resistors 10, 11 of predetermined values and outputs the resulting signal.

[0004]

10 Further, the AM receiver converts the signal wave S_{AF} detected by the detection circuit 8 converts to a DC voltage V_{AGC} via a low pass filter 9 to obtain a constant (non-variable) signal wave S_{AF}.

[0005]

15 Assuming the amplification ratio of the gain control intermediate frequency amplifier 6 is fixed, a variation in the amplitude of the AM broadcast wave S_{RF} in accordance with a variation in the receiving intensity causes a variation in the signal wave S_{AF} even in case the AM broadcast wave S_{RF} of

20 the same detection data level is detected.

[0006]

In order to prevent such a disadvantage, a constant (non-variable) signal wave S_{AF} is obtained by lowering the amplification ratio of the gain control intermediate frequency

25 amplifier 6 when a DC voltage V_{AGC} is raised, and by raising

2

the amplification ratio of the gain control intermediate frequency amplifier 6 when the DC voltage V_{AGC} is lowered.

[0007]

[Problems that the Invention is to Solve]

The inventor of the application has replaced a received composed of the aforementioned analog circuits with one composed of digital circuits to make an attempt to directly regenerate the digital signal wave S_{AF} that is compatible with for example digital audio apparatus.

[0008]

More precisely, the inventor has digitized a receiver itself, without providing an additional feature whereby an analog signal wave S_{AF} output from the detection circuit 8 in Fig. 3 is converted to a digital signal wave via an A/D converter, thus directly outputting a digital signal wave S_{AF}. The inventor, in doing so, has attempted to develop a more high-accuracy receiver that was not available via an analog receiver.

[0009]

The inventor, as one of such attempts, has proposed to implement high-accuracy signal processing obtained through digital arithmetic operation, by replacing the gain control intermediate frequency amplifier 6, the noise clamping circuit 7 and the low pass filter 9 with digital circuits.

[0010]

The proposal presented a problem. While frequency of

3

each signal supplied to the gain control intermediate frequency amplifier 6, the noise clamping circuit 7 and the low pass filter 9 is down-converted to an intermediate frequency (455 kHz) via the frequency conversion in the frequency converter 3, the

5   frequency is too high for general digital circuits to process. This requires introduction of extremely high-speed digital circuits, not just replacement of existing circuits.

[0011]

In order to perform the digital signal processing

10   equivalent to that in the gain control intermediate frequency amplifier 6, the noise clamping circuit 7 and the low pass filter 9 as analog circuits according to the related art, it is necessary to digitize the IF signal S_{IF} output from the band-pass filter at a sampling frequency at least double the intermediate

15   frequency (455 kHz), for example a sampling frequency of 1 MHz according to the Nyquist sampling theorem.

[0012]

Thus, there was a problem that high-speed and expensive digital circuits were required, which made it difficult to

20   digitize a receiver.

[0013]

For example, an approach for high-speed digital signal processing provides a plurality of digital circuits that can perform high-speed arithmetic operation in parallel and

25   implements substantial high-speed arithmetic operation through

parallel processing using these plurality of digital circuits. This approach requires complicated control for obtaining precise synchronization between digital circuits and invites high costs due to expanded circuit scale.

5 [0014]

The invention aims at solving the problems involved in the related art and providing a new receiver of a simple configuration that can directly output high-accuracy digital signal waves.

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SUMMARY OF THE INVENTION

[0015]

[Means for Solving the Problems]

The invention, in order to attain the object, proposes
15 a receiver for regenerating a signal wave from a received wave that is amplitude-modulated, characterized in that the receiver comprises a variable gain control means for performing variable gain adjustment of detection data generated by detection of the received wave that is frequency-converted to an intermediate
20 frequency signal to detection data having a constant level via digital signal processing, and a noise clamping means for performing noise clamping of the detection data having a constant level output from the variable gain control means via digital signal processing.

25 [0016]

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According to such a configuration, the variable gain control means and the noise clamping means perform digital signal processing on detection data having a frequency lower than that of the intermediate frequency signal. Thus, it is possible

5 to configure variable gain control means and noise clamping means without applying high-speed digital circuits and to implement a new receiver of a simple configuration that can directly output high-accuracy digital signal waves.

[0017]

10 The receiver is characterized in that the variable gain control means comprises a digital low pass filter for integrating detection data to generate DC component data, a digital divider for dividing predetermined first reference data to indicate a detection data level by the DC component data generated by

15 the digital low pass filter, and a digital multiplier for multiplying division data output from the digital divider via the division by the detection data to generate the detection data having a constant level.

[0018]

20 According to the configuration, division data corresponding to a variation in the detection data is generated when the digital divider divides the DC component data by the predetermined first reference data, and the detection data having a constant level is generated when the digital multiplier

25 multiplies the division data and the detection data. This

implements a so-called AGC circuit for keeping detection data constant via digital signal processing irrespective of a variation in detection data.

[0019]

5   The receiver is characterized in that the noise clamping means comprises a digital comparator for comparing predetermined second reference data to indicate a clamp level with the detection data having a constant level and outputting the comparison results, and a selector circuit for outputting

10   the detection data having a constant level as the data for the signal wave when the detection data having a constant level is smaller than the second reference data, and outputting the second reference data as the data for the signal wave when the detection data having a constant level is larger than the second

15   reference data.

[0020]

According to such a configuration, even in case a large noise exceeding the detection data level is superimposed on the detection data having a constant level output from the

20   variable gain control means, the detection data having a constant level with the noise removed is generated.

[0021]

The receiver is further characterized in that the receiver comprises a digital multiplier for multiplying the first

25   reference data by a predetermined scale factor so that the second

reference data is generated.

[0022]

According to such a configuration, setting just the first reference data generates the second reference data of a predetermined scale factor. This simplifies operation for data setting.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of a receiver according to the embodiment.

Fig. 2 shows the operation of a digital multiplier provided in the receiver according to the embodiment.

Fig. 3 is a block diagram showing a configuration of a receiver for regenerating a signal wave from a broadcast wave via the analog signal processing according to the related art.

DEITALED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023]

[Mode for Carrying Out the Invention]

An embodiment of the invention will be described referring to drawings. Fig. 1 is a block diagram showing a configuration of a receiver according to the embodiment. In this embodiment is shown a receiver for receiving AM broadcast waves.

[0024]

The receiver in Fig. 1 supplies an AM broadcast wave S_{RF}

8

received via an antenna 12 to a frequency converter 14 via a high-frequency amplifier 13, mixes the resulting signal with a channel selection signal S_o of the local oscillation frequency from a local oscillator 15 in order to frequency-convert the signal to an IF signal S_{IF} of the intermediate frequency (455 kHz), removes unwanted frequency components by passing the IF signal S_{IF} through a band-pass filter 16 in the intermediate frequency band, then detects the signal via a detection circuit 17 to generate a detection signal in the audio frequency band.

[0025]

The high-frequency amplifier 13, the frequency converter 14, the band-pass filter 16 and the detection circuit 17 are formed of analog circuits.

[0026]

Following the detection circuit 17 are serially connected an AGC (Automatic Gain Control) circuit AGCC as variable gain control means and a noise clamping circuit NCC as noise clamping means.

[0027]

Although not shown, an A/D converter is provided whereby the detection signal generated by the detection circuit 17 is sampled at a sampling frequency about double the audio frequency band (for example about 100 Hz to 20 kHz), for example a sampling frequency of 41 kHz to convert the detection signal to digital data (hereinafter referred to as detection data) D1. Detection

9

data D1 output from the A/D converter is supplied to the AGC circuit AGCC.

[0028]

The AGC circuit AGCC is composed of a digital multiplier 18, a digital low pass filter 19, and a digital divider 20.

[0029]

The digital low pass filter 19 inputs detection data D1 and outputs DC voltage data D2 indicating a DC voltage proportional to the detection data D1 via digital filtering.

[0030]

The digital divider 20 inputs DC voltage data D2 and reference detection level data D3 mentioned later, then performs division of data D2 by D3. The digital divider 20 supplies division data D4 obtained through the division to the digital multiplier 18, as shown in Expression (1).

[0031]

[Expression 1]

$$D4 = (K \times D2) \div 3 \qquad \ldots (1),$$

where the coefficient K in Expression 1 is a proportion coefficient (constant) used by the digital low pass filter 19 for generating DC voltage data D2 by performing digital filtering (integration) on the detection data D1 based on a predetermined constant.

[0032]

The digital multiplier 18 multiplies the detection data

D1 and the division data D4 and outputs the multiplication data D5 obtained via the multiplication to the noise clamping circuit NCC.

[0033]

The noise clamping circuit NCC is composed of a digital comparator 23 and a selector circuit 24.

[0034]

The digital comparator 23 compares the value of the multiplication data D5 and the preset voltage data D6 mentioned later and outputs the comparison data D_{cmp} as a comparison result. In case the value of the multiplication data D5 is smaller than the preset voltage data D6 (D5<D6), the digital comparator 23 outputs comparison data D_{cmp} that is logically '1'. In case the value of the multiplication data D5 is equal to or larger than the preset voltage data D6 (D5≧D6), the digital comparator 23 outputs comparison data D_{cmp} that is logically '0'.

[0035]

The selector circuit 24 is composed of a so-called data multiplexer where multiplication data D5 is input to a first input terminal A, preset voltage data D6 is input to a second input terminal B, and comparison data D_{cmp} is input to a select terminal SEL. When the comparison data D_{cmp} is logically '1', the selector circuit 24 outputs the multiplication data D5 from an output terminal Q. When the comparison data D_{cmp} is logically '0', the selector circuit 24 outputs the preset voltage data

11

D6 from the output terminal Q. That is, the selector circuit 24 selects between the multiplication data D5 and the preset voltage data D6 according to the logical value of the comparison data D_{cmp}, and outputs the selected data as signal wave data D_{AF}.

[0036]

The receiver is equipped with a register circuit 21, a multiplier 22 formed of a shift register, and a controller 25 having a microprocessor (MPU).

[0037]

The controller 25 supplies reference data D_{set} for setting the maximum span of the signal wave data D_{AF} to the register circuit 21. The register circuit 21 maintains the reference data D_{set} and supplies the reference data D_{set} as reference detection level data D3 to the divider 20 and the multiplier 22.

[0038]

The multiplier 22 is formed of for example a parallel-input parallel-output shift register. The multiplier 22, as shown in Fig. 2, outputs preset voltage data D6 that has a value equal to an integral multiple of the reference detection level data D3, by inputting the reference detection level data D3 and shifting the entire input data toward the higher bits by arbitrary number of bits.

[0039]

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Fig. 2 illustrates a case where the preset voltage data D6 that equals a value of decimal '200' is output by shifting the reference detection level data D3 when the data D3 is set to decimal '100'.

5 [0040]

As detailed later, setting the detection level data D3 to decimal '100' causes the processing to be performed corresponding to the detection data level '100'.

[0041]

10 Operation of the receiver having such a configuration according to the embodiment will be described below.

In the product inspection process of a receiver, an inspector operates the controller 25 to preset the reference data D_{set} then performs product shipment. The inspector sets,

15 for example, a value of decimal '100' to specify a detection data level of '100'.

[0042]

When the user turns on the receiver and the antenna 12 receives a broadcast wave from a broadcast station, the AM

20 broadcast wave S_{RF} is high-frequency-amplified by the high-frequency amplifier 13, and mixed with the channel selection signal S_o of the local oscillation frequency from the local oscillator 15 by the frequency converter 14 so that the resulting signal is frequency-converted (down-converted) to

25 an IF signal S_{IF} of the intermediate frequency (455 kHz). The

13

IF signal S_{IF} then passes through the band-pass filter 16 in the intermediate frequency band, detected by the detection circuit 17 to become a detection signal in the audio frequency band, converted to digital detection data D1 by the A/D converter that is not shown, then supplied to the AGC circuit AGCC.

[0043]

In the AGC circuit AGCC, the digital low pass filter 19 generates DC voltage data D2 indicating a DC voltage proportional to the detection data D1. The digital divider 20 performs division of the DC voltage data D2 by the reference detection level data D3 from the register circuit 21 and supplies the resulting division data D4 to the digital multiplier 18. The digital multiplier 18 multiplies the detection data D1 by the division data D4 to generate and output multiplication data D5 $(=D1 \times D4)$.

[0044]

Note that the multiplication data 5 is kept constant even in case the detection data D1 varies with the receiving intensity of the AM broadcast wave S_{RF}.

[0045]

For example, when the value of the detection data D1 (amplitude value) has changed to a value of decimal '40' in case reference detection level data D3 is set to decimal '100', the value of DC voltage data D2 becomes "40×K', division data D4 becomes D4=2.5×K, and multiplication data D5 becomes D5=100

14

×K, all in proportion to the variation in the value of detection data D1, as shown in Expression (2).

[0046]

In case the value of the detection data D1 (amplitude value) has changed to a value of decimal '80', data D2, D4, and D5 have values as shown in Expression (3).

[0047]

In case the value of the detection data D1 (amplitude value) has changed to a value of decimal '160', data D2, D4, and D5 have values as shown in Expression (4).

[0048]

[Expression 2]

$D3=100$

$D1=40$

$D2=40\times K$ $\qquad\}\ ...(2)$

$D4=D3\div D2=100\div(40\times K)=2.5\times K$

$D5=D1\times D4=40\times(2.5\times K)=100\times K$

[0049]

[Expression 3]

$D3=100$

$D1=80$

$D2=80\times K$ $\qquad\}\ ...(3)$

$D4=D3\div D2=100\div(80\times K)=1.25\times K$

$D5=D1\times D4=80\times(1.25\times K)=100\times K$

[0050]

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[Expression 4]

D3=100

D1=160

D2=160×K   } ...(4)

D4=D3÷D2=100÷(160×K)=0.625×K

D5=D1×D4=160×(0.625×K)=100×K

In this way, even in case the detection data D1 has varied with the receiving intensity of the AM broadcast wave S_{RF}, the AGC circuit AGCC performs gain control via digital signal processing to always keep constant and output the multiplication data D5.

[0051]

Next, when the multiplication data D5 is supplied to the noise clamping circuit NCC, the digital comparator 23 compares the value of the multiplication data D5 and the preset voltage data D6 from the digital multiplier 22. The digital multiplier 22 supplies preset voltage data D6 indicating '200', double the reference detection level data D3 via the aforementioned bit shift.

[0052]

Via such a configuration, in case D5<D6, comparison data D_{cmp} that is logically '1' is supplied to the selector circuit 24, and in case D5≧D6, comparison data D_{cmp} that is logically '0' is supplied to the selector circuit 24. Depending on the logical value of the comparison data D_{cmp}, the selector circuit

16

24 selectively outputs multiplication data D5 or preset voltage data D6 to generate signal wave data D_{AF}.

[0053]

In case an external noise that exceeds the detection data level '200' determined by the preset voltage data D6 is superimposed on the multiplication data D5, the preset voltage data D6 is output as signal wave data D_{AF}. Otherwise, the multiplication data D5 is output as signal wave data D_{AF}.

[0054]

Thus, the noise clamping circuit NCC is configured to generate signal wave data D_{AF} with noises suppressed via digital signal processing.

[0055]

In this way, according to the embodiment, configuring the AGC circuit AGCC and the noise clamping circuit NCC via digital circuits can provide a receiver that regenerates and directly outputs digital signal wave data D_{AF}.

[0056]

In this configuration, a detection signal in the audio frequency range output from the detection circuit 17 is converted to detection data D1 by the A/D converter that is not shown, and the detection data D1 undergoes digital signal processing via the AGC circuit AGCC and the noise clamping circuit NCC. Thus it is not necessary to form the A/D converter, the AGC circuit AGCC and the noise clamping circuit NCC via high-speed

digital circuits, thus preventing high costs for the receiver design.

[0057]

That is, in case the gain control intermediate frequency amplifier 6, the noise clamping circuit 7 and the low pass filter 9 of the receiver in Fig. 2 described as the related art are replaced with digital circuits, it is necessary to process digital data at a sampling frequency at least double the intermediate frequency, for example a sampling frequency of 1 MHz considering an aliasing error in order to support the IF signal S_{IF} of the intermediate frequency (455 kHz). Thus it is necessary to provide high-speed digital circuits. However, according to the embodiment, since a detection signal in the audio frequency range (for example 100 Hz to 20 kHz) is processed, the sampling frequency ca be set to as low as 41 kHz considering so-called reproducibility of a signal with an aliasing error suppressed, thereby eliminating the need for supplying high-speed digital circuits.

[0058]

In case high-speed digital circuits according to the related art are applied, such problems arise that digital circuits are more complicated and high-accuracy and complicated synchronization control between digital circuits is required between digital circuits. According to the embodiment, low-speed digital signal processing is made possible thus

18

eliminating the need for high-accuracy and complicated synchronization control and simplifying the circuit scale, thereby preventing high costs for the receiver design.

[0059]

5   In the product inspection process of a receiver, an inspector has only to preset the reference data D_{set} to the controller 25 to automatically determine the reference detection level data D3 that indicates the detection data level and the preset voltage data D6. This simplifies inspection

10   and adjustment work as well as considerably reduces human errors such as misadjustment.

[0060]

For example, in a receiver shown in Fig. 2, adjusting the detection level of the detection circuit 8 involves

15   adjustment of the clamp level of the noise clamping circuit 7. This complicates the adjustment work thus easily causing human errors. According to the embodiment, such a drawback can be considerably offset.

[0061]

20   While the embodiment assumes a case where the preset voltage data D6 double the reference detection level data D3 is automatically set when the digital multiplier 22 performs single-bit shift processing, the digital multiplier 22 may perform double-bit shift processing. Addition/subtraction of

25   n-bit-shifted arbitrary data to/from m-bit-shifted arbitrary

19

data may be used to automatically set an arbitrary value. For example, a combination of bit shift and addition/subtraction mat be used where addition of 1-bit-shifted arbitrary data to -1-bit-shifted arbitrary data is used to automatically set an arbitrary value.

[0062]

While the embodiment assumes a case where the value of the reference data D_{set} is set to decimal '100' corresponding to a detection data level of '100', the value of the reference data D_{set} may be set arbitrarily.

[0063]

While a digital multiplier 22 according to the embodiment generates preset voltage data D6 having a value equal to an integral multiple of the reference detection level data D3 by bit-shifting the reference detection level data D3 in order to further simplify the configuration of the receiver, a digital multiplier that performs multiplication without using the bit-shift processing.

[0064]

For example, it is possible to supply multiplicand attribute data for specifying a scale factor from the controller 25 to the digital multiplier that performs multiplication without using the bit-shift processing and the digital multiplier may multiply the multiplicand attribute data by the reference detection level data D3 to generate the preset voltage

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data D6.

[0065]

While the embodiment of an AM receiver for receiving a broadcast wave coming from a broadcast station is described, the invention is not limited to a receiver that regenerates a signal wave based on a broadcast wave.

[0066]

While the embodiment assumes that circuits up to the detection circuit 17 are configured by analog circuits, the invention is not limited to this configuration. Any receiver that comprises an AGC circuit a noise clamping circuit that perform digital signal processing and falls within the scope of the invention.

[0067]

[Advantages of the Invention]

As mentioned earlier, according to the invention, the variable gain control means and the noise clamping means perform digital signal processing on detection data having a frequency lower than that of the intermediate frequency signal. Thus, it is possible to configure variable gain control means and noise clamping means without applying high-speed digital circuits and to provide a new receiver of a simple configuration that can directly output high-accuracy digital signal waves.

[0068]

The variable gain control means comprises a digital low

21

pass filter for integrating detection data to generate DC component data, a digital divider for dividing predetermined first reference data by the DC component data generated by the digital low pass filter, and a digital multiplier for multiplying

5   division data output from the digital divider via the division by the detection data to generate detection data having a constant level. This implements a so-called AGC circuit for keeping detection data constant via digital signal processing irrespective of a variation in detection data.

10 [0069]

The noise clamping means comprises a digital comparator for comparing the size of the detection data having a constant level with that of predetermined second reference data that indicates a clamp level, and a selector circuit for outputting

15 the detection data having a constant level as the data for the signal wave when the detection data having a constant level is smaller than the second reference data, and outputting the second reference data as the data for the signal wave when the detection data having a constant level is larger than the second

20 reference data. Thus, even in case a large noise exceeding the clamp level is superimposed on the detection data having a constant level, the detection data having a constant level with the noise removed is generated.

[0070]

25 The receiver comprises a digital multiplier for

22

multiplying the first reference data by a predetermined scale

factor so that the second reference data is generated.   Thus,

setting just the first reference data generates the second

reference data of a predetermined scale factor.   This simplifies

5   operation for data setting.